IN THE CLAIMS:

1. (Previously Presented) A method for issuing instructions in a multithreaded computer processor, the method comprising the steps of:

receiving a set of computer instructions in an instruction issue logic, wherein each instruction of said set comprises one instruction from each of a plurality of independent instruction threads;

identifying as dependent instructions those received instructions that require a result from a prerequisite instruction;

determining a probability for each received instruction that the received instruction will complete all stages of a multi-stage instruction pipeline of the processor without causing a stall, wherein the probability for each received instruction is expressed as a percentage value;

selecting the received instruction of the set that is least likely to cause a stall in the multi-stage pipeline; and

issuing the selected instruction into the pipeline for processing, from the instruction issue logic, when the probability for the selected instruction is above a predetermined threshold that is 50%.

2. (Previously Presented) The method of claim 1, further comprising the step of: determining whether there is a shared resource conflict between two or more of the received instructions of the set.

3. (Previously Presented) The method of claim 2, further comprising the step of: resolving a given one of said shared resource conflicts between two or more of said received instructions, after said given conflict has been discovered.

4. (Cancelled)

5. (Previously Presented) The method of claim 1, further comprising:

predicting a stage, within the multi-stage instruction pipeline, where results of each instruction will be available, and said step of determining the probability for a received instruction includes calculating a critical distance comprising a number of stages between a stage when the received instruction will need a given result, and a stage when a result will be available.

6. (Previously Presented) The method of claim 5, wherein the probability for a dependent instruction is determined based upon a current location and a predicted stage of any prerequisite instruction and upon a predicted resolution of any identified shared resource conflict.

7. (Previously Presented) The method of claim 6, further comprising the step of:

dynamically recalculating the probability for each instruction based on current contents of the pipeline and a current status of any shared resources.

8.- 30. (Cancelled)

31. (Previously Presented) A method for issuing instructions in a multithreaded computer processor, comprising the steps of:

receiving a set of computer instructions in an instruction issue logic, wherein each set of instructions comprises one instruction from each of a plurality of independent instruction threads;

predicting a stage, within a multi-stage instruction pipeline of the computer processor, where results of each instruction will be available;

identifying as dependent instructions those received instructions that require a result from a prerequisite instruction;

calculating a critical distance comprising a number of stages between a stage when a selected dependent instruction will need a given result, and a stage when the result will be available;

determining whether the selected instruction is within a critical distance, and if so, determining a probability that the selected instruction will complete all stages of the pipeline without causing a stall, wherein said probability is expressed as a percentage value; and,

issuing the selected instruction into the pipeline for processing, from the instruction issue logic, when the probability is above a predetermined threshold that is 50%.

32.-40. (Cancelled)